Microwave-Circuit Modeling of High Lead-Count Plastic Packages

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***Abstract*— A microwave-circuit model topology for elevated-paddle surface-mount packages is extended to packages with high-lead counts. Features such as irregular lead structures, long wirebonds, smaller pitches, and finite-lead thickness are all examined. The modeling technique is applied to a shrink small-outline package (SSOP-24) with the results compared to measurements of a 25 times size scale model. The circuit model is used to investigate the performance of a matched transition.**

I. Introduction

SURFACE-MOUNT plastic packages are widely used for low-cost microwave integrated circuits. Such packages come in various types, sizes, and grounding schemes. The most inexpensive packages are those used also by low-frequency integrated-circuit (IC) vendors. They consist of a conducting paddle which is surrounded by an array of leads, which suspend the paddle above the printed circuit motherboard to which the package mounts. Some of these leads connect the paddle to the motherboard ground plane through vias in the motherboard substrate. A monolithic microwave integrated circuit (MMIC) is soldered, and the paddle and wirebonds connect its input, output, and power pads to the appropriate members of the lead array. The characteristics that make the elevated paddle packages so difficult to use at microwave frequencies are: 1) the lead inductance separating the MMIC ground from the motherboard ground; 2) the lack of good circuit models for such packages; and 3) the lack of attention to the grounding pattern on the motherboard substrate.

In this paper, we will describe a circuit model developed for use with a 24-lead surface-mount shrink small-outline package (SSOP). The model topology has been described in [1] for an 8-lead small-outline IC (SOIC) package. Extending the model to an SSOP-24 package requires dealing with a number of complicating features. Some aspects of the model were outlined in [2], but lack of space precluded a detailed description. Fig. 1 illustrates a top view of the paddle plane for such a package. In contrast to the SOIC-8, the SSOP-24 uses three times more leads, the leads are irregularly shaped, and there are long leads located at the paddle ends. Furthermore, the bond wires can be long and slant away from the originating leads. The methods adopted to tackle these problems were not discussed in [1]. Also, the lead modeling in previous work assumes a lead thickness of zero in order to use a three-dimensional (3-D) planar solver, **em**.[1] In this paper, we use a full 3-D solver, HFSS[2] for the lead simulations, and compare the results to those obtained from the planar assumption. We also compare our circuit-model results to measurements of a scaled-model SSOP-24 package, especially noting the package related detuning effects and reduced isolation.

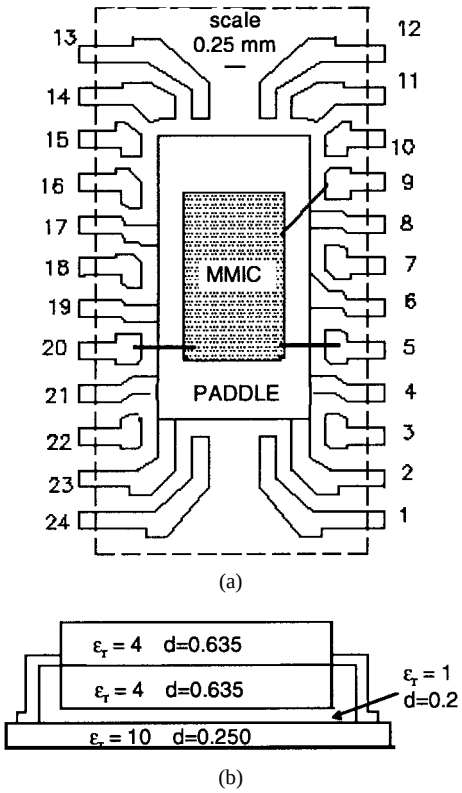

Fig. 1. (a) Top view of paddle plane. (b) Side view of package and substrate layers.

In this paper, the model, measurements, and an application are presented. In Section II, we outline the model and present the method for determining it for the 24-lead SSOP. Scale-model measurements are compared to the circuit-model simulations in Section III. The model is applied to investigate the characteristics of a matched transition in Section IV.

II. Circuit Model

Fig. 2 shows the circuit topology of the model. It consists of three pieces: a paddle model, a lead model, and the inter-

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[1] **em** is a trademark of Sonnet Inc., Liverpool, NY.

[2] HFSS is a trademark of Hewlett-Packard, Santa Rosa, CA.

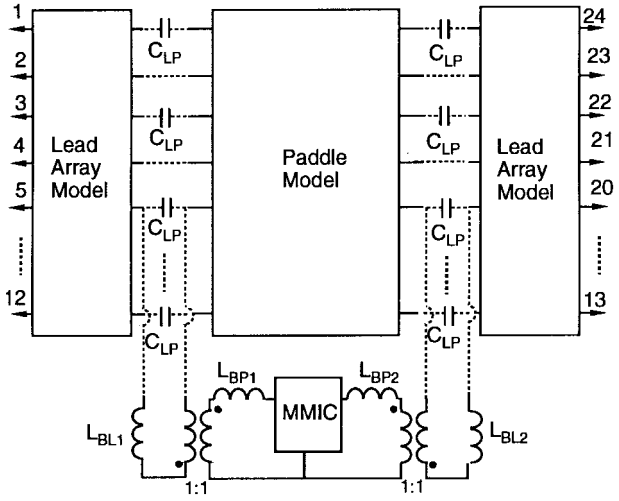

Fig. 2. Circuit topology for modeling elevated-paddle surface-mount packages. The topology corresponds to a first-cut modeling of the package illustrated in Fig. 1, except that leads 6–11 and 14–19 are omitted for simplicity.

connection modeling. A user connects these pieces with each other and with the MMIC model in whatever way is optimal for the design. A circuit model is separately developed for each piece based on the results of an electromagnetic simulation. By simulating separately, we assume that each piece couples to the other only through the terminal connections we show. This assumption has been verified by comparisons to full simulations and to measurements.

Important parts of the model are the ideal 1:1 transformers, one of which is used for each connection crossing from a lead to the MMIC. They and the paddle model control the way the currents returning from the MMIC find their way to the motherboard ground plane. The physical justification for this scheme is presented in [1] and will not be repeated here.

A. Paddle Model

We simulate the way the paddle distributes ground return currents by placing microstrip ports along the paddle perimeter and determining the y-parameters of the resulting multiport. Usually a port is located on the paddle perimeter opposite the location of a lead. In the fully assembled package model, some of these ports will be connected to motherboard ground through the lead array. The other ports are left open or are connected to a transformer, as shown in Fig. 2. The transformer's purpose is to force a return current to the proper port on the paddle model.

Fig. 3 shows the layout for the **em** simulation of the paddle. The dielectric layered structure above and below the paddle is the same as the paddle sees in the actual package, including the air gap between the motherboard and the package. One exception is that in the actual package, the dielectric stops just beyond the paddle edge, whereas in the simulation it extends across the entire simulation box. Normally, each paddle port has a width roughly equal to the width of the nearby lead. In the SSOP-24 case, paddle ports associated with leads 3, 10, 15, and 22 are omitted as unnecessary since their positions on the paddle perimeter are very close to the ports associated

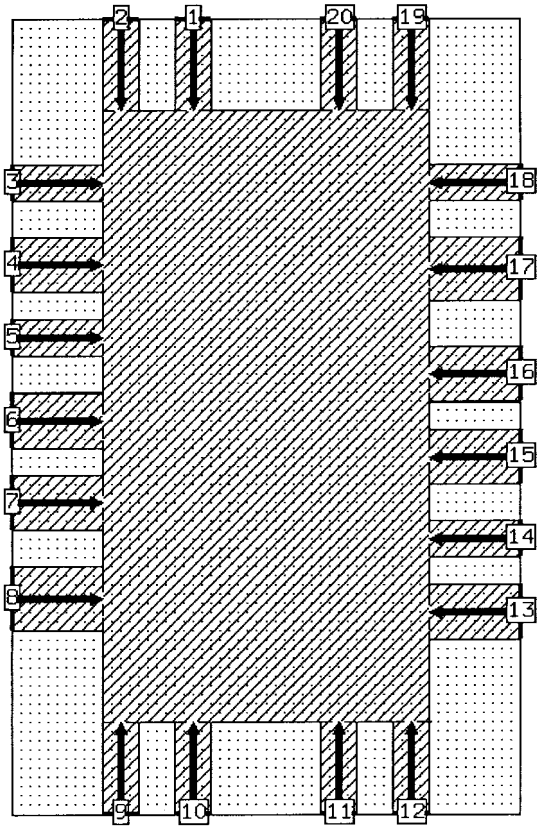

Fig. 3. Layout for **em** simulation of the paddle.

with leads 2, 11, 14, and 23. In fact, the modeling becomes inaccurate if perpendicular port reference planes touch each other as they would if 3, 10, 15, and 22 were included. The 20-port y-parameters were obtained from simulations at 2.5 GHz (double precision). A full 3-D simulation could have been used for the paddle modeling, but the planar simulation is sufficiently accurate and is much faster.

The circuit model for the paddle consists of 20 nodes, one at each port, which are interconnected with inductors determined from the simulated y-parameters according to

$$L(i,j) = \frac{-1}{j\omega y_{ij}} \tag{1}$$

where $L(i,j)$ is the inductance between nodes i and j, and y_{ij} is the admittance obtained from simulation [3]. In addition, each node will have a capacitance to ground given by

$$C_p = \frac{1}{j\omega N z_{ii}} \tag{2}$$

where i corresponds to any one of the ports, and N is the number of paddle ports.

Based on the simulator results, we note that the transfer admittance will be largest between adjacent nodes. We adopt the strategy that an inductor connecting nodes i and j will be eliminated if $|y_{ij}| < 0.08 \min(y_{i,i+1}, y_{j,i-1}, y_{i,j+1}, y_{j,j-1}), j > i$. Some of the smaller admittances are somewhat sensitive to paddle asymmetry and this has resulted in some odd omissions. For example, the admittance $y_{1,3}$ is neglected, but the admittance $y_{10,8}$ is included. Table II in the Appendix

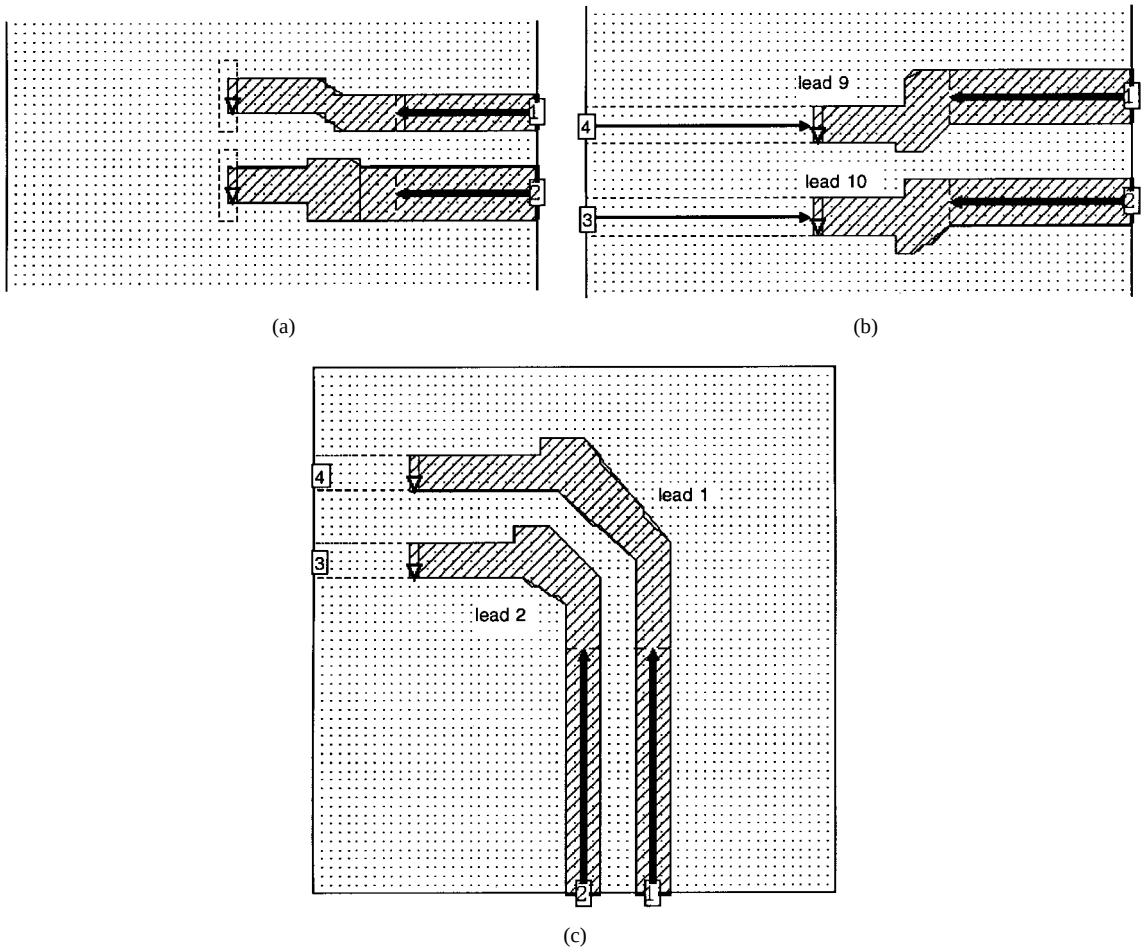

Fig. 4. Simulator layout on the paddle plane of (a) grounding leads 4 and 5, (b) nongrounding leads 9 and 10, and (c) nongrounding leads 1 and 2.

lists the values of the various inductances in the model and C_p. Some of the inductances between nonadjacent nodes are negative. These are unphysical artifacts of the simplified model. As stated above, the circuit model was determined from simulated y-parameters at 2.5 GHz. We compared the model to **em** simulations at 15 GHz and found agreement to within 5% for the self and transfer admittances. The behavior of the paddle y-parameters is approximately inductive over the frequency range of interest. C_p improves the accuracy of the circuit model at higher frequencies.

B. Lead Modeling

The basic procedure for modeling the leads of the SSOP-24 configuration is the same as in [1]. However, it is complicated by the presence of leads on all four sides of the paddle and the variety of configurations for the lead pattern near the paddle. We first classify leads into two categories—grounding and nongrounding leads. One end of a grounding lead connects with the paddle at the paddle level. The other end connects to the motherboard ground plane through a via that is located directly beneath the point where the lead touches the motherboard surface (see Fig. 1). The nongrounding leads do not touch the paddle, and thus are shorter at the paddle end (by 0.25 mm) than the grounding lead. At the other end, the nongrounding leads connect to microstrip feeds located on the motherboard top surface. We further subdivide these two categories into leads located on the broad side of the paddle and those at the ends of the paddle. The leads on the ends are much longer than the broadside leads, and the circuit model for them had to be modified.

Fig. 4 shows the **em**-simulation patterns used to generate models for leads in the categories described above. Fig. 4(a) and (b) show pairs of grounded and nongrounded broadside leads. Fig. 4(c) shows an example of nongrounded-end leads. The planar simulation used here is good for modeling the experimental structure that will be described in the following section, but it is not accurate enough for modeling the thick leads used in an actual plastic package.

Fig. 5 shows the general topology of the circuit model for the leads. For simplicity, we neglect the coupling between nonadjacent leads. The model elements are found by simulating one pair of leads at a time. For example, consider leads 9 and 10 in Fig. 4(b) and label ports 1–4 in a clockwise fashion. At low frequencies (1 GHz) the simulated y-parameters are primarily inductive and can be used to find $L(9)$, $L(10)$, and $M(9,10)$ from

$$L(9) = \frac{y_{22}}{j\omega\left(y_{11}y_{22} - y_{12}^2\right)} \tag{3}$$

$$L(10) = \frac{y_{11}}{j\omega\left(y_{11}y_{22} - y_{12}^2\right)} \tag{4}$$

$$M(9,10) = -\frac{y_{12}}{y_{22}}L(9). \tag{5}$$

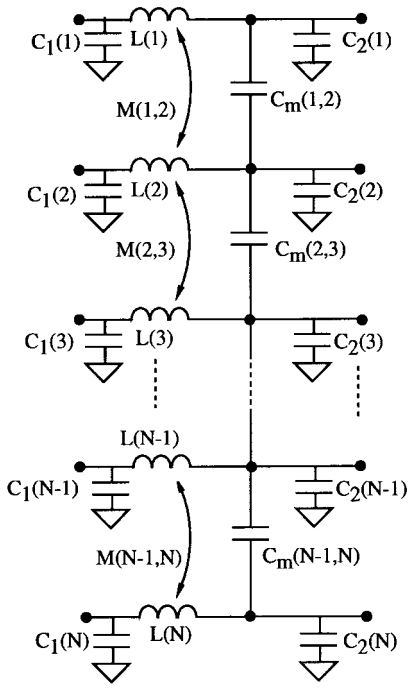

Fig. 5. Circuit model for lead array.

At higher frequencies, capacitive effects become more important and we use the deviation of the y-parameters from inductive behavior to find the self and mutual capacitances. The resulting formulas are

$$C_1(9) = \frac{\omega_H y_{44}|_{\omega_H} - \omega_L y_{44}|_{\omega_L}}{j\left(\omega_H^2 - \omega_L^2\right)} \tag{6}$$

$$C_2(9) + C_m(9,10) = \frac{\omega_H y_{11}|_{\omega_H} - \omega_L y_{11}|_{\omega_L}}{j\left(\omega_H^2 - \omega_L^2\right)} \tag{7}$$

$$C_m(9,10) = \frac{\omega_H y_{12}|_{\omega_H} - \omega_L y_{12}|_{\omega_L}}{-j\left(\omega_H^2 - \omega_L^2\right)} \tag{8}$$

where the high and low frequencies correspond to 4 and 1 GHz. For grounded leads such as those in Fig. 4(a), the corresponding left-hand ports of the circuit model are grounded and C_1 is eliminated. Equations (7) and (8) are used to obtain C_2 and C_m.

The inductance connecting the paddle to the motherboard ground has a very crucial effect on the performance of the package. This inductance depends on the inductance of the package lead, the inductance of the motherboard grounding via, and the inductance of any microstrip line on the motherboard surface that connects the two. It is tempting to simply sum the inductances of these three pieces, but this neglects the mutual coupling between them, specifically between the vertical section of the package lead and the via. When the via is directly under the lead, this mutual coupling is especially important and the via and lead should be simulated as one unit. For example, the simulated inductance of a vertical strip of width 0.4 mm and length 0.8 mm connecting to ground through a via 0.25 mm long is low by about 15% if the inductance of the vertical section and the via are determined separately and added.

The nongrounding leads on either end of the package are significantly longer than those along the broad side. These long leads have a more distributed nature. For best accuracy, we found it necessary to supplement the mutual capacitor C_m with another mutual capacitor C_{mm} connecting between adjacent leads on the motherboard side of the circuit model (the left side of Fig. 5). This makes it a little more complicated to find the capacitances from the simulated network parameters. Using leads 1 and 2 in Fig. 4(c) as an example, label the ports clockwise starting from the lower right corner. At low frequencies, where capacitive effects dominate the z-parameters of the network we get

$$C_m(1,2) + C_{mm}(1,2) = \frac{z_{12}}{j\omega\left(z_{11}z_{22} - z_{12}^2\right)} \tag{9}$$

$$C_1(1) + C_2(1) = \left(C_m(1,2) + C_{mm}(1,2)\right) \times \left(\frac{z_{11}}{z_{12}} - 1\right) \tag{10}$$

$$C_1(2) + C_2(2) = \left(C_m(1,2) + C_{mm}(1,2)\right) \times \left(\frac{z_{22}}{z_{12}} - 1\right) \tag{11}$$

where the z-parameters were determined at 1 GHz (The z-parameter subscripts refer to the port numbers, not the lead numbers). We need three more relations which we take from the y-parameters:

$$C_2(1) + C_m(1,2) - C_1(1) - C_{mm}(1,2) = (y_{11} - y_{44})/(j\omega) \tag{12}$$

$$C_2(2) + C_m(1,2) - C_1(2) - C_{mm}(1,2) = (y_{22} - y_{33})/(j\omega) \tag{13}$$

$$C_m(1,2) - C_{mm}(1,2) = (y_{34} - y_{12})/(j\omega). \tag{14}$$

The y-parameters in this case were taken from simulations at a higher frequency of 4 GHz, since for example, y_{11} and y_{44} are very nearly equal at lower frequencies.

We have used both the 3-D planar method-of-moments solver **em** and the full 3-D FEM-solver HFSS to find the y- and z-parameters noted above. In our verification studies, we have compared the circuit-model results to a full-wave **em** simulation of a packaged test circuit and to measurements of a scale model (only the latter is presented in this paper). For those cases, it has been satisfactory to assume zero-thickness conductors, and **em** was most convenient. However, in a real SSOP package, the lead width is nominally 0.25 mm and the thickness is 0.15 mm. The lead pitch is 0.635 mm, which gives a nominal edge-to-edge separation of 0.385 mm. With these dimensions, a zero-conductor thickness assumption is questionable. **em** can simulate finite-thickness conductors using vertical blocks of expansion currents; however, we use the full 3-D FEM-simulator HFSS for that purpose.

Table I compares selected component values for the package in Fig. 1, determined from three different simulations: a planar MoM simulation (**em**), a planar FEM simulation (zero thickness conductors in HFSS), and a full 3-D FEM simulation (HFSS). The results from the first and second

TABLE I
MODEL COMPONENTS (PICOFARAD AND NANOHENRY) FOR SELECTED GROUNDING LEADS AS DETERMINED FROM THREE TYPES OF SIMULATIONS. ALL GROUNDING LEADS INCLUDE THE MOTHERBOARD VIA GROUND INDUCTANCE

	MoM Planar Simulation	FEM Planar Simulation	FEM 3-D Simulation
$L(1)$	2.10	2.03	1.60
$L(2)$	1.51	1.45	1.12
$M(1,2)$	0.47	0.48	0.46
$C_2(2)$	0.043	0.047	0.052
$C_2(1)$	0.070	0.073	0.082
$C_m(1,2)$	0.035	0.041	0.056
$L(4)$	1.23	1.16	0.83
$L(5)$	1.16	1.11	0.81
$M(4,5)$	0.37	0.31	0.26
$C_2(4)$	0.031	0.034	0.049
$C_2(5)$	0.039	0.046	0.059
$C_m(4,5)$	0.021	0.022	0.043

simulation methods should be the same, and the table shows that they deviate by only several percent in most cases. The component values obtained from the full 3-D simulation (including conductor thickness) are substantially different. The self-inductance terms determined from planar simulation are about 30–70% larger than the self inductances obtained from 3-D simulation. The mutual inductances (capacitances) from planar simulation are about 40%–50% larger (smaller) than those from 3-D simulation. The self capacitances from planar simulation were 20%–50% smaller than those obtained from 3-D simulation. So accurate modeling of these packages must take into account the thickness of the leads.

The 3-D simulations also allow us to model the irregular dielectric structure of the package, whereas the planar analysis in **em** must assume dielectric layers that extend across the entire computational box. However, we found that this had little effect.

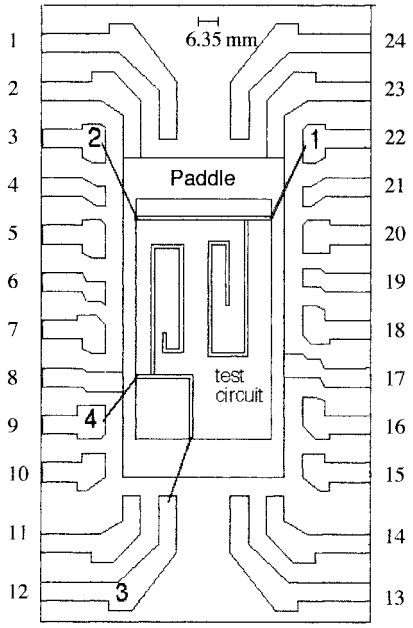

Fig. 6. Top view of paddle plane for approximate 25 times scale model of SSOP-24 package.

A listing of the lead model components derived from HFSS results can be found in the Appendix.

C. Interconnect Modeling

The components in Fig. 2 that interconnect the lead model, paddle, and MMIC are the ideal transformer, the wirebond inductances, and the lead-to-paddle capacitance $C_{\rm lp}$.

We divide the wirebond inductance into two parts, one for the wirebond section passing over the paddle $(L_{\rm BP})$ and one for the section extending between the paddle edge and the lead to which the wire bonds $(L_{\rm BL})$. The current in the part of the wirebond passing over the paddle causes an oppositely directed image current to flow on the paddle back toward the paddle edge where the wirebond originally crossed. From there it flows along the paddle edges until it can pass through the grounding leads to the motherboard ground. We determine the inductance of the paddle wirebond section from simulation of a wire which is elevated above a ground plane [4], [5] by the average height of the wire over the paddle. The other wirebond section has its image (return) current located much farther away, and thus, the image has much less effect. In the work described here, the wirebond from the lead to the paddle edge is modeled as a wire elevated above the motherboard ground plane. Also, in simulating the nonpaddle wirebond, we connect the feedline for the simulation to the wirebond at right angles in order to eliminate the added apparent inductance that mutual coupling with the feed would normally provide. We do this under the assumption that mutual coupling between the paddle wirebond and the nonpaddle wirebond is canceled by the nearby image current in the paddle. On the lead side of the nonpaddle wirebond section, we keep the feed in line with the wirebond in order to roughly approximate the mutual coupling between the wirebond and the lead to which the wirebond connects.

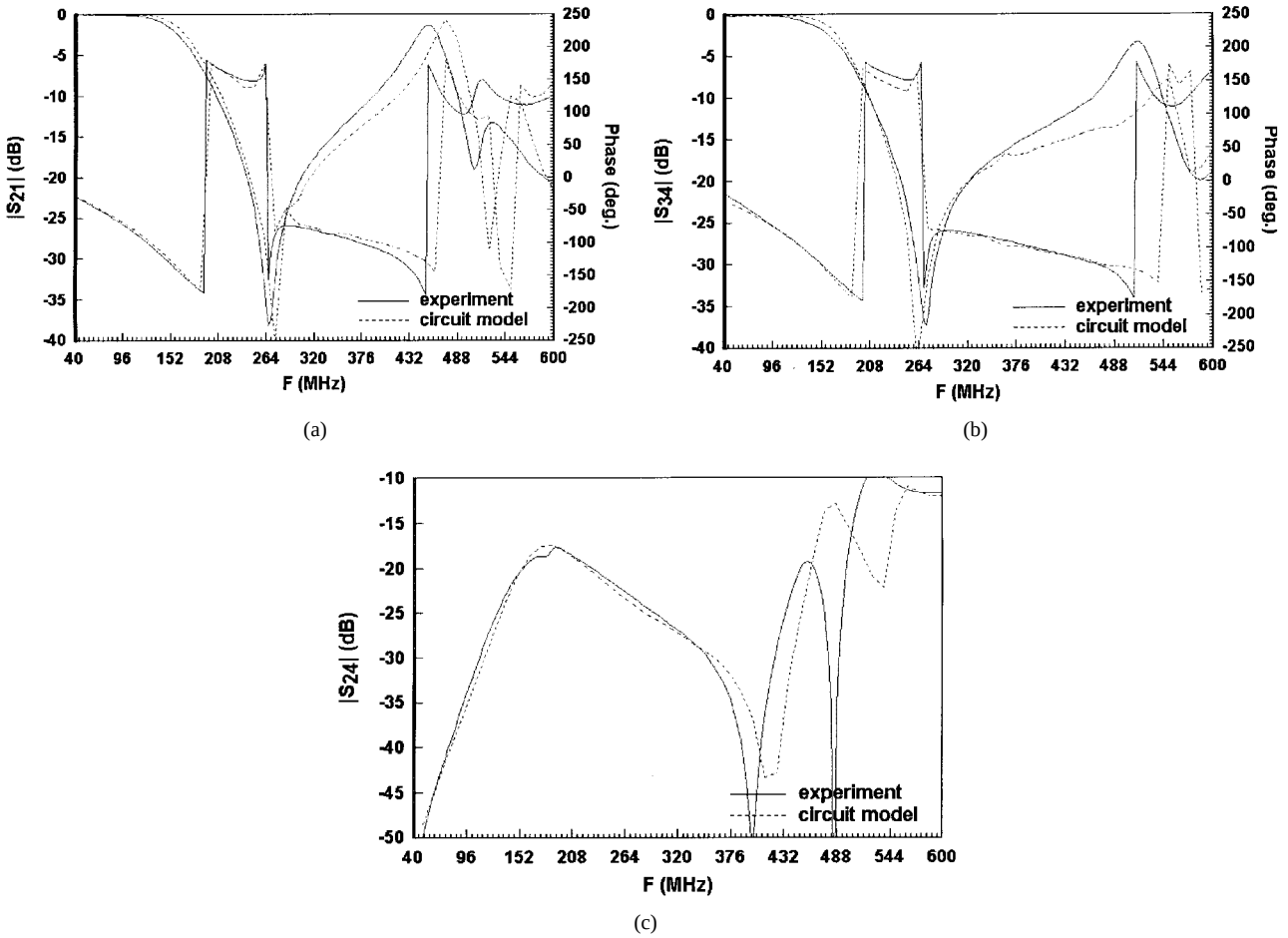

Fig. 7. Comparison of the circuit simulation to measured scale model for (a) S_{12}, (b) S_{34}, and (c) $|S_{24}|$.

The connection of the transformer in the model depends upon the routing of the wirebond in the physical package. One transformer terminal on the paddle side always connects to the MMIC ground. One transformer terminal on the lead side connects to the paddle model port that is associated with the point on the paddle edge closest to where the paddle image return current hits the edge of the paddle. Consider lead nine in Fig. 1 as an example. The transformer return should connect to the paddle port opposite lead eight (port seven in Fig. 3) since the wirebond crosses closest to that paddle port.

The capacitance between the leads and the paddle $C_{\rm lp}$ can also be significant, especially at frequencies near a package resonance. To determine $C_{\rm lp}$, we simulate on HFSS a two-port gap circuit consisting of a microstrip on one side having a width consistent with the end of a lead and on the other side a very wide microstrip. The gap between the two is the same as the lead paddle gap in the physical package (0.25 mm). We found this capacitance to be about 50 fF for leads that end in a narrow pad and 80 fF for leads that end in a wide pad.

III. Measurements of a Scale Model

To verify the circuit model, we compared our circuit-model results to full-wave simulations of an entire package with a test circuit enclosed. Very good agreement was observed [1], [6]. For brevity, we do not present those results in this paper. Instead, we present comparisons of the circuit-model simulations to measurements of a scale-model package.

We fabricated a scale model of the SSOP-24 package. Wherever practical, all dimensions of the model were 25 times actual size. The model consisted of a paddle pattern etched (see Fig. 6) on one surface of a 0.125-in Duroid substrate with a dielectric constant of 2.2. All of the conductor was removed from the bottom side of this substrate. The paddle substrate was supported above a motherboard substrate by leads formed from 0.25-in-wide brass strips bent to the proper shape and soldered to the paddle. A test MMIC chip (consisting of a 0.050-in Duroid substrate with a dielectric constant of 10.8) was etched to create the microstrip test patterns shown in Fig. 6 and silver epoxied to the paddle. The motherboard was created from another 0.125-in Duroid substrate $(\varepsilon_r = 2.2)$. Input and output 50-Ω microstrip feed lines were etched on its top surface, and the paddle/lead assembly soldered to them. Leads 2, 8, 17, and 23 were soldered to grounding vias consisting of 0.187-in flat-head brass bolts located directly beneath the vertical lead sections. The remaining leads are omitted entirely. For ease of fabrication, the model differs from an exact scale in that the dielectric constants are different and the conductor and dielectric thicknesses are much less than an exact scaling would make them. Nevertheless, the essential elements of an SSOP-24 package remain. The experimental structure was circuit modeled as it exists and not by modeling

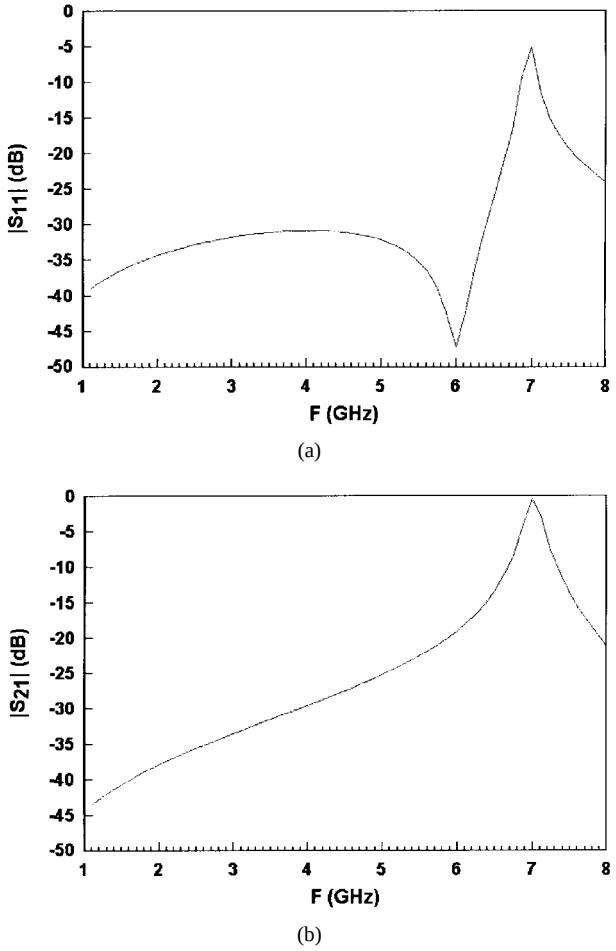

Fig. 8. Simulation results of a matched transition (a) $|S_{11}|$ with 50-Ω on-chip termination and (b) $|S_{21}|$ with short circuits as on-chip terminations.

an actual package and multiplying each element by the scale factor. Measurements were taken from 40 to 600 MHz which scales up to 1.0–15 GHz.

As illustrated in Fig. 6, the microstrip test circuits each consist of a 50-Ω through line with a long open-circuit stub connected in shunt. The stub on the line connecting port one (lead 22) and port two (lead three) becomes a quarter-wavelength long at 280 MHz, thus causing a transmission zero at that frequency. The through/stub connecting between port three (lead 12) and port four (lead nine) has a transmission zero at 380 MHz. The package will shift these transmission zeros and cause a loss of isolation between the two circuits. The circuit model should predict these effects.

Fig. 7(a) show the magnitude and phase of S_{21}, measured and modeled. Note that modeled results track the measurements up to and past the first package resonance at 460 MHz (scales to 11.5 GHz). The modeled transmission zero occurs at 275 MHz and the measured transmission zero is at 270 GHz. Note from Fig. 6 that this circuit has grounding leads near to its input and output leads. As a result, the circuit is well grounded and the package has little effect on the transmission zero.

Fig. 7(b) shows S_{34} measured and modeled. In this case, packaging the circuit has shifted the transmission zero down from 380 to 275 MHz. This is due to the fact that no paddle

TABLE II
INDUCTANCE (IN NANOHENRY) NETWORK MODELING THE PADDLE PATTERN IN FIG. 3. IN ADDITION TO THESE INTER-NODE INDUCTANCES, A SHUNT CAPACITANCE OF $C_p = 0.0147$ pF CONNECTS EACH NODE TO GROUND

L(1,2)=0.134	L(1,4)=1.7	L(1,20)=0.252
L(2,3)=0.080	L(2,4)=-0.45	L(2,5)=-1.5
L(3,4)=0.096	L(3,18)=-0.86	
L(4,5)=0.092	L(4,6)=-1.7	
L(5,6)=0.108	L(5,7)=-1.5	
L(6,7)=0.094	L(6,8)=-1.6	
L(7,8)=0.110	L(7,9)=-0.97	
L(8,9)=0.200	L(8,10)=1.6	
L(9,10)=0.136	L(9,11)=-2.1	
L(10,11)=0.252	L(10,12)=-2.2	
L(11,12)=0.137	L(11,13)=1.9	
L(12,13)=0.163	L(12,14)=-0.80	
L(13,14)=0.089		
L(14,15)=0.108	L(14,16)=-1.5	
L(15,16)=0.094	L(15,17)=-1.5	
L(16,17)=0.131	L(16,19)=-1.6	
L(17,18)=0.097	L(17,19)=-0.41	L(17,20)=1.6
L(18,19)=0.080		
L(19,20)=0.134		

grounding lead is near to port three and the return current must take a long circuitous route to return to beneath the microstrip feed. The package circuit model properly predicts the shift in the zero to within 4% of measurement. This example verifies the circuit model for a poor grounding situation. It also illustrates the importance of ground-lead location.

The magnitude of S_{42} is a measure of the isolation between the two circuits. Simulations show that $|S_{42}|$ is less than -40 dB in the unpackaged case. However, Fig. 8 shows that the package causes the isolation to deteriorate a very great deal, with $|S_{42}|$ peaking at -14 dB for 180 MHz (equivalent to 4.5 GHz unscaled). The circuit model closely tracks the measurement up to 340 MHz (equivalent to 8.5 GHz unscaled) and then roughly tracks it up to the package resonance.

IV. WIDE-BAND TRANSITION

The circuit model described above will now be used to investigate a wide-band transition from a microstrip motherboard feed to a packaged MMIC. This can be done by including a single shunt capacitance on the MMIC at the point where RF connections are made. To determine the proper shunt capacitance, we use the circuit model described in Section II with the finite-thickness lead model listed in the Appendix. Assuming that a 50-Ω match is desired, we put a 50-Ω load in place of the MMIC input in Fig. 2. The matching capacitance is put in shunt with it. In this particular case, we used lead five as a signal lead and leads four and six as paddle grounds. We connect another 50-Ω termination with a shunt matching capacitor (through a second ideal transformer) to lead 18 with leads 17 and 19 grounding the paddle. The signal leads plus their adjacent ground leads form a transition structure similar to a coplanar waveguide. All other leads are connected to the motherboard ground, but not connected to the paddle other than through the parasitic capacitances $C_{\rm lp}$. The motherboard substrate assumed here is 0.25-mm thick with an $\varepsilon_r = 10$. All connections to the motherboard ground are through vias directly beneath the feet of the leads. We optimized the value of the shunt capacitance in order to minimize the reflection seen from the motherboard over the largest frequency range

TABLE III
COMPONENT VALUES FOR THE CIRCUIT MODEL OF LEAD 1–12 IF THE LEADS ARE USED TO GROUND THE PADDLE. ALL INDUCTANCES INCLUDE THE MOTHERBOARD VIA GROUND INDUCTANCE. ALL UNITS ARE IN PICOFARAD AND NANOHENRY. ENTRIES IN PARENTHESES REFER TO LEAD(S) WHICH ARE SIMILAR ENOUGH TO SUBSTITUTE. LEADS 11 AND 12 ARE NOT USED FOR GROUNDING

$Lead_i$	L(i)	M(i,i+1)	C_2(i)	C_m(i,i+1)
1	1.6	0.46	0.082	0.056
2	1.12	0.40	0.052	0.081
3	(5)	(5,6)	(5)	(5,6)
4	0.83	0.26	0.049	0.043
5	0.81	0.26	0.059	0.041
6	(4)	(4,5)	(4)	(4,5)
7	0.89	0.26	0.059	0.052
8	0.80	(7,8)	0.071	(7,8)
9	(5)	(4,5)	(5)	(4,5)
10	(5)	(2,3)	(5)	(2,3)
11	N/A	N/A	N/A	N/A
12	N/A	N/A	N/A	N/A

TABLE IV
COMPONENT VALUES FOR THE CIRCUIT MODEL OF LEAD 1–12 IF THE LEADS ARE NOT USED TO GROUND THE PADDLE. ALL UNITS ARE IN PICOFARAD AND NANOHENRY. ENTRIES IN PARENTHESES REFER TO LEAD(S) WHICH ARE SIMILAR ENOUGH TO SUBSTITUTE. N/A IS NOT APPLICABLE AND NGL INDICATES ASSUMED NEGLIGIBLE

$Lead_i$	L(i)	M(i,i+1)	C_1(i)	C_2(i)	C_m(i,i+1)	C_{mm}(i,i+1)
1	1.36	0.39	0.18	0.12	0.083	0.081
2	0.85	0.28	0.13	0.054	0.067	N/A
3	(10)	(5,6)	(10)	(10)	(5,6)	N/A
4	0.54	(5,6)	0.13	0.038	(5,6)	N/A
5	0.52	0.18	(9)	(9)	0.029	N/A
6	(4)	(5,6)	(4)	(4)	(9,10)	N/A
7	(9)	(9,10)	(9)	(9)	(9,10)	N/A
8	(4)	(5,6)	(4)	(4)	(9,10)	N/A
9	0.49	0.17	0.21	0.049	0.027	N/A
10	0.50	(2,3)	0.21	0.038	(2,3)	N/A
11	0.68	0.32	0.15	0.036	0.086	0.015
12	1.18	ngl	0.23	0.076	ngl	ngl

possible. This resulted in a capacitance of 0.13 pF for the lead five transition and 0.12 pF for the lead 18 transition.

Fig. 8(a) shows a plot of the circuit simulated reflection as seen from the foot of lead five. Return loss of greater than 30 dB is predicted up to 6.4 GHz. At 7 GHz, a package resonance occurs. This resonance is sensitive to the number of grounding leads and also the capacitive connection between the paddle and the unconnected leads C_{lp}. If we reduce C_{lp} by a factor of four (by increasing the gap from lead to paddle), this resonance moves up to 8 GHz, and the return loss remains over 30 dB up to 8 GHz.

The transition investigated above gives a good match, but it is also important that the package provide good isolation. Fig. 8(b) shows the transmission between the lead five-port and the lead 18-port if the 50-Ω loads on the paddle plane are replaced by shorts to paddle ground. The isolation is better than 25 dB up to 5 GHz. Connecting two more ground leads (leads 2 and 23) to the paddle moves the resonance from 7 to 8 GHz and extends the 25-dB isolation to 7.3 GHz.

Measurements of a wide-band transition similar to this one on an SOIC-8 scale-model package have shown good agreement with the model and return losses better than 25 dB up to the scaled equivalent of 6 GHz.

V. CONCLUSION

A three-piece package model has been applied to a 24-lead plastic-SSOP package. The complexities of modeling such a package have been described. These include long irregularly shaped leads and long wirebonds that cross to the packaged MMIC at oblique angles. The necessity of using a 3-D simulator for modeling the leads has been investigated and typical lead model values listed. Circuit simulator results have been compare to measurements of an approximate scale-model package showing good agreement up to the first package resonance at the scaled equivalent of 11 GHz. The model was applied to the design of a very simple matched transition that had a simulated return loss of better than 30 dB up to 6.4 GHz.

An important feature of this model is that it correctly predicts that packaged circuit performance depends on paddle ground location and not only the number of grounding leads.

APPENDIX

Tables II, III, and IV list the component values for the paddle and lead models for the approximate SSOP-24 package illustrated in Fig. 1. The paddle-model components result from the simulation of the pattern in Fig. 3. The lead-model results from HFSS simulations and are only listed for leads 1–12. Leads 13 through 24 are similar.

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Robert W. Jackson (M'82–SM'88), for a photograph and biography, see this issue, p. 1925.

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